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EXAMINER

ALI, SYED J

ART UNIT PAPER NUMBER

2195

DATE MAILED: 05/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/934,443

Applicant(s)

LANDMAN ET AL.

Examiner

Syed J. Ali

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 04 March 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-6 and 9-32 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-6 and 9-32 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 04 March 2005 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

1. This office action is in response to the amendment filed March 4, 2005. Claims 1-6 and 9-32 are presented for examination.
2. The text of those sections of Title 35, U.S. code not included in this office action can be found in a prior office action.

Claim Rejections - 35 USC § 101

3. **Claims 1-6, 9-10, 15-20, and 27-32 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.**
4. As per claims 1, 15, 18, 27, and 30, the claimed apparatus, data structure, and systems are software per se, as they are not tangibly embodied on any sort of physical medium. The claims recite a "processing element", but this limitation is described as being software in the specification (pg. 6 lines 20-22, "A processing element [PE] may be, for example, a single computer, a cluster of coupled computers, *or one of several tasks, each task being run in a multitasking environment on a single computer.*") (emphasis added).

The claims have been amended to indicate that the apparatus and systems of claims 1, 18, and 27 are "*implemented in a computer-readable medium.*" However, even if the apparatus, data structure, and/or systems are implemented in a computer-readable medium, the apparatus, data structure, and systems are still wholly embodied within software. There is no hardware or physical medium recited as part of the apparatus, data structure, or systems themselves.

Claims 2-6, 9-10, 16-17, 19-20, 28-29, and 31-32 are rejected for similar reasons as discussed for their respective parent claims, as they fail to present any limitations that resolve the deficiencies of the claims from which they depend.

Claim Rejections - 35 USC § 102

5. **Claims 1-6, 9-15, 17-19, 21-31 are rejected under 35 U.S.C. 102(b) as being anticipated by Blleloch et al. (USPN 5,768,594) (hereinafter Blleloch).**

6. As per claim 1, Blleloch teaches the invention as claimed, including an apparatus, implemented in a computer-readable medium, for subdividing input data associated with a software program and processing each subdivided input data on one or more processing elements, comprising:

a non-threaded initiating program (col. 2 lines 14-27);

one or more non-threaded processing programs (col. 2 lines 57-63); and

a wrapper that intercepts a call to the initiating program and operable to subdivide input parameters into one or more job quanta (col. 3 lines 13-19), wherein each job quantum is submitted for execution to a separate processing program selected from the one or more processing programs residing on a separate processing element (col. 5 lines 15-30).

7. As per claim 2, Blleloch teaches the invention as claimed, including the apparatus of claim 1, wherein the wrapper assembles one or more output data from each processing program to form a single results data (col. 2 lines 44-46; col. 2 line 64 - col. 3 line 5).

8. As per claim 3, Blleloch teaches the invention as claimed, including the apparatus of claim 1, wherein each job quantum is provided to a separate job scheduler residing on each of the processing elements, each scheduler manages the execution of the processing program executing on the processing element (col. 2 lines 57-63).

9. As per claim 4, Blleloch teaches the invention as claimed, including the apparatus of claim 1, further comprising:

one or more additional wrappers, each additional wrapper residing on a single processing element and is operable to intercept the job quantum submitted to the processing program residing on the processing element (col. 2 lines 57-63; col. 3 lines 20-38).

10. As per claim 5, Blleloch teaches the invention as claimed, including the apparatus of claim 1, wherein the initiating program and each of the processing programs perform one or more operations that are substantially identical (col. 2 lines 28-43).

11. As per claim 6, Blleloch teaches the invention as claimed, including the apparatus of claim 5, wherein the operations are bioinformatic calculations (col. 2 lines 14-27).

12. As per claim 9, Blleloch teaches the invention as claimed, including the apparatus of claim 1, wherein at least one of the processing elements resides in a disparate processing environment from the initiating program (col. 2 lines 28-37).

13. As per claim 10, Blelloch teaches the invention as claimed, including the apparatus of claim 1, wherein the input parameters are normalized prior to being subdivided into the job quanta (col. 2 lines 14-27).

14. As per claim 11, Blelloch teaches the invention as claimed, including a method of processing a non-threaded set of executable instructions, comprising:

receiving input data associated with a call to a first non-threaded set of executable instructions (col. 2 lines 14-27; col. 3 lines 13-19);

parsing the input data into a plurality of job quanta, each job quantum operable to be independently processed by the first non-threaded set of executable instructions (col. 3 lines 13-19); and

submitting at least one job quantum for execution to a second non-threaded set of executable instructions that is substantially identical to the first non-threaded set of executable instructions (col. 2 lines 28-43; col. 5 lines 15-30), wherein the second set of executable instructions resides on one or more different processing elements from the first non-threaded set of executable instructions (col. 2 lines 28-37).

15. As per claim 12, Blelloch teaches the invention as claimed, including the method of claim 11, further comprising:

assembling an output data associated with the results of the execution of the second non-threaded set of executable instructions for a presentation (col. 2 lines 44-46; col. 2 line 64 - col. 3 line 5).

16. As per claim 13, Blleloch teaches the invention as claimed, including the method of claim 11, further comprising:

submitting at least one job quantum for execution to the first non-threaded set of executable instructions (col. 5 lines 15-30).

17. As per claim 14, Blleloch teaches the invention as claimed, including the method of claim 13, wherein the executions occur substantially in parallel (col. 2 lines 14-27).

18. As per claim 15, Blleloch teaches the invention as claimed, including a job quanta data structure, comprising:

a first data (col. 3 lines 13-19; Fig. 1);

a second data wherein the first and second data are operable to be delineated and independently submitted as input parameter data used for execution by a separate non-threaded sets of executable instructions and processed substantially in parallel on different processing elements (col. 3 lines 13-19; Fig. 1).

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19. As per claim 17, Blleloch teaches the invention as claimed, including the job quanta of claim 15, wherein the first and second data are initially submitted as input parameter data to a single non-threaded set of executable instructions (col. 2 lines 14-27).

20. As per claim 18, Blleloch teaches the invention as claimed, including a system, implemented in a computer-readable medium, for performing parallel processing on a call to execute a software program, comprising:

means for intercepting a call to the software program, which is non-threaded (col. 2 lines 14-27; col. 3 lines 13-19);

means for dividing a set of input data into a plurality of job quanta including a first job quantum and a second job quantum (col. 3 lines 13-19);

means for submitting the first job quantum to the software program and for submitting the second job quantum to a separate software program (col. 3 lines 13-19); and

means for executing the software program and the separate software programs substantially in parallel (col. 2 lines 14-27).

21. As per claim 19, Blleloch teaches the invention as claimed, including the system of claim 18, further comprising:

means for assembling output data associated with the execution of the software program and at least one of the separate software programs into a presentation data (col. 2 lines 44-46; col. 2 line 64 - col. 3 line 5).

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22. As per claim 21, Blleloch teaches the invention as claimed, including a method of processing a software program, comprising:

receiving input data associated with a call to the software program, which is non-threaded (col. 2 lines 14-27; col. 3 lines 13-19);

parsing the input data into a plurality of job quanta, each job quantum operable to be independently processed by the software program (col. 3 lines 13-19); and

submitting at least one job quantum for execution to a replica software program that is substantially identical to the software program (col. 2 lines 28-43; col. 5 lines 15-30), wherein the replica software program resides on one or more different processing elements from the software program (col. 2 lines 28-37).

23. As per claim 22, Blleloch teaches the invention as claimed, including an information handling system, comprising:

a network (col. 2 lines 47-56);

a plurality of processing elements (col. 2 lines 47-56);

memory operatively coupled to the processing elements (col. 2 lines 47-56); and

means for wrapping a call to a non-threaded application program by dividing input data among the processing elements for execution according to the application program (col. 3 lines 13-19; col. 5 lines 15-30) and recombining output data from the processing elements (col. 2 lines 44-46; col. 2 line 64 - col. 3 line 5).

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24. As per claim 23, Blleloch teaches the invention as claimed, including a method of processing a set of executable instructions, comprising:

receiving input data associated with a call to the set of executable instructions, which are non-threaded (col. 2 lines 14-27; col. 3 lines 13-19);

separating the input data into a plurality of job quanta, wherein each job quantum is operable to be independently processed by the set of executable instructions (col. 3 lines 13-19);
and

submitting at least one job quantum for execution to a substantial copy of the set of executable instructions, and submitting a different job quantum to the set of executable instructions (col. 2 lines 28-43; col. 5 lines 15-30), wherein the substantial copy of the set of executable instructions and the set of executable instructions reside on different processing elements (col. 2 lines 28-37).

25. As per claim 24, Blleloch teaches the invention as claimed, including the method of claim 23, further comprising assembling output data from the execution of the substantial copy of the set of executable instructions and from the set of executable instructions into a single presentation data (col. 2 lines 44-46; col. 2 line 64 - col. 3 line 5).

26. As per claim 25, Blleloch teaches the invention as claimed, including the method of claim 23, further comprising executing the substantial copy of the set of executable instructions and the set of executable instructions substantially in parallel (col. 2 lines 14-27).

27. As per claim 26, Blleloch teaches the invention as claimed, including the method of claim 23, wherein in separating the input data, the input data is separated into the plurality of job quanta by a wrapper associated with the set of executable instructions (col. 3 lines 13-19).

28. As per claim 27, Blleloch teaches the invention as claimed, including a parallel processing system, implemented in a computer-readable medium, comprising:

a first software program having a wrapper operable to intercept calls made to the first software program (col. 2 lines 14-27; col. 3 lines 13-19), wherein the first software program resides on one or more first processing elements and is non-threaded (col. 2 lines 28-37);

a second software program which is a substantial copy of the first software program and which is non-threaded, wherein the second software program resides on one or more second processing elements (col. 2 lines 28-37); and

wherein the wrapper intercepts the calls and parses input data associated with the calls into job quanta, the job quanta includes a first job quantum and a second job quantum (col. 3 lines 13-19; col. 5 lines 15-30), and the first job quantum is submitted to the first software program for processing and the second job quantum is submitted to the second software program for processing substantially in parallel (col. 2 lines 14-27).

29. As per claim 28, Blleloch teaches the invention as claimed, including the system of claim 27, wherein the wrapper assembles output results associated with the processing of the first job quantum and the second job quantum (col. 2 lines 44-46; col. 2 line 64 - col. 3 line 5).

30. As per claim 29, Blelloch teaches the invention as claimed, including the system of claim 27, wherein one or more of the first processing are different from one or more of the second processing elements (col. 2 lines 28-37).

31. As per claim 30, Blelloch teaches the invention as claimed, including a parallel processing system, comprising:

a wrapper that intercepts calls to non-threaded software programs (col. 2 lines 14-27; col. 3 lines 13-19), wherein the software programs are substantial copies of each other and reside on different processing elements (col. 2 lines 28-43; col. 2 lines 28-37), and wherein the wrapper separates input data associated with the calls into a plurality of independent job quanta (col. 3 lines 13-19); and

a scheduler that receives the plurality of job quanta from the wrapper and submits substantially in parallel different job quantum associated with the job quanta to a number of the software programs for processing (col. 2 lines 14-27; col. 3 lines 13-19), wherein the scheduler selects the number of the software programs based on processing loads associated with the number of software programs (col. 3 lines 20-30).

32. As per claim 31, Blelloch teaches the invention as claimed, including the system of claim 30, wherein the wrapper assembles results associated with processing the different job quantum for a unified presentation (col. 2 lines 44-46; col. 2 line 64 - col. 3 line 5).

Claim Rejections - 35 USC § 103

33. **Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Blelloch in view of Shah et al. (US 2002/0035556) (hereinafter Shah).**

34. As per claim 16, Shah teaches the invention as claimed, including the job quanta of claim 15, wherein the first and second data are delineated using extensible markup language (paragraph 0076).

35. It would have been obvious to one of ordinary skill in the art to combine Blelloch and Shah since the distribution of processing across multiple machines may include distributing processing to machines that are incompatible. XML provides a format that is platform independent and allows specific custom functionality to be provided, thereby making it a highly desirable format for encapsulating data that is to be distributed amongst a diverse group of machines.

36. **Claims 20 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Blelloch in view of Klein (USPN 6,185,590).**

37. As per claim 20, Klein teaches the invention as claimed, including the system of claim 19, further comprising:

means for trapping and reporting error conditions generated by the execution of the software program and at least one of the separate software programs (col. 6 lines 7-11).

38. It would have been obvious to one of ordinary skill in the art to combine Blelloch and Klein for the purpose of protecting against improper engine functioning and providing a method of handling errors. When distributing processing across multiple computers to compute a shared result, one processing element's failure would lead to a total failure in the corresponding output. Encapsulating a way of identifying errors makes it so that one processing element's failure is not propagated to all the other processing elements' output as well.

39. As per claim 32, Klein teaches the invention as claimed, including the system of claim 30, wherein the scheduler traps any errors associated with processing the different job quantum and reports the errors to the wrapper (col. 6 lines 7-11).

Response to Arguments

40. **Applicant's arguments filed March 4, 2005 have been fully considered but they are not persuasive.**

41. Applicant argues that Blelloch "*assumes that the initial program or programs being processed are in fact already threaded. Blelloch is dedicated to taking a threaded program and scheduling its execution with multiple parallel processing elements.*" Applicant later adds, "*there is no teaching in Blelloch that could even remotely support non-threaded programs that are also processed by different processing elements.*"

42. Examiner respectfully disagrees with Applicant's characterization of Blelloch. Blelloch is specifically concerned with the problem of providing a concurrent or parallel processing

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environment for sequential tasks (col. 1 lines 12-17, 35-43; col. 2 lines 14-27). A sequential program is, by definition, non-threaded. There may be data dependencies or benefits achieved by parallel processing, but the program itself is initially non-threaded. The program is then divided up into sub-tasks and assigned to different processing elements, such that the program can be processed in less time. In fact, Blleloch discusses how a sequential program can be manipulated into emulating a threaded program. The program codes that indicate the location of data dependencies and ordering of instructions are passed to the scheduler to ensure that the sub-tasks are properly ordered (col. 3 lines 39-44). Furthermore, Blleloch discusses the use of status buffers that enable tasks to manage their dependencies, such that a task that is dependent on data from another task is stalled until that data is available (col. 3 lines 20-38). Had the tasks actually been threaded, as alleged by Applicant, there would be no need for such a status buffer; the data dependencies could be handled by a synchronization construct or mutex.

43. Applicant argues that “*Examiner has interpreted the Assignment Manager [AM] [with respect to claim 7’s rejection] to be a non-threaded program, since the AM is listed in column 4 lines 28-29 as performing function in ordinary sequence.*” Applicant points out other portions of Blleloch, e.g. col. 4 lines 26-28, as allegedly forming the basis for the rejection.

44. The rejection does not rely upon the portion of Blleloch identified in Applicant’s argument. Furthermore, Applicant has canceled claim 7. These factors alone are enough to render the argument moot. Nonetheless, Examiner has not relied upon the AM as being any of the claimed non-threaded programs; the AM determines which tasks need to be processed and then distributes the tasks to the processing elements. Whether the AM is threaded or non-

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threaded has no implications upon whether the incoming program or the processing elements are threaded or non-threaded. Applicant is invited to re-read the rejection and the reference, as there seems to be a misunderstanding as to which portions of Blleloch relate to the program being processed, the processing elements performing the processing, and the programs that assign the program to be processed to the processing elements.

45. Applicant argues, *“Examiner is again trying to use the AM of Blleloch as a catchall capable of a variety of conflicting things. The AM of Blleloch is either threaded in which case it processes on processing elements or it is not threaded in which case the tasks of the initial program are what are processed on the processing elements. Neither of these two interpretations support the conclusion that Applicants claim 11 is anticipated.”*

46. Applicant has mischaracterized the rejection. The AM is not relied upon as any sort of catchall. The claimed invention discusses dividing a non-threaded application into “job quanta” and assigning these quanta to various processing elements. The AM is an intermediary that performs the assignment. It does not perform processing on processing elements, nor is it the task being processed. Applicants argument with respect to the AM has no bearing on whether the incoming program is threaded or non-threaded.

Conclusion


47. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Syed J Ali whose telephone number is (571) 272-3769. The examiner can normally be reached on Mon-Fri 8-5:30, 2nd Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai T An can be reached on (571) 272-3756. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).


Syed Ali
May 13, 2005


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